US 20180137815A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2018/0137815 A1**

CHENG (43) **Pub. Date: May 17, 2018**

(54) **PIXEL CIRCUIT AND ELECTROLUMINESCENT DISPLAY COMPRISING THE PIXEL CIRCUIT**

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(21) Appl. No.: **15/439,420**

(22) Filed: **Feb. 22, 2017**

Related U.S. Application Data

(60) Provisional application No. 62/421,435, filed on Nov. 14, 2016.

Publication Classification

(51) **Int. Cl.**

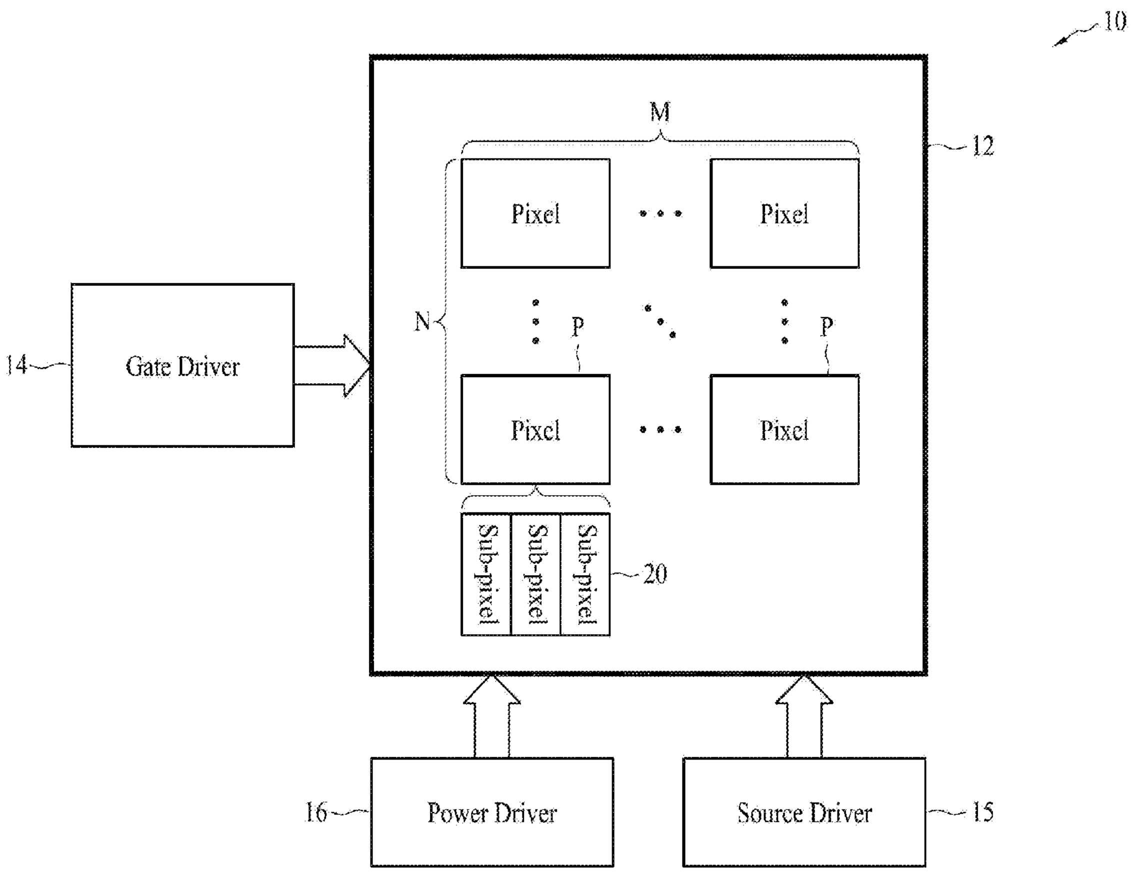
G09G 3/3233	(2006.01)
H01L 27/32	(2006.01)
H01L 51/50	(2006.01)

(52) **U.S. Cl.**

CPC ***G09G 3/3233*** (2013.01); ***H01L 27/3211*** (2013.01); ***H01L 27/3248*** (2013.01); ***H01L 51/5036*** (2013.01); *G09G 2310/0278* (2013.01); *G09G 2300/0452* (2013.01); *G09G 2300/043* (2013.01); *G09G 2300/0814* (2013.01); *G09G 2300/0842* (2013.01); *G09G 2300/0443* (2013.01)

(57) **ABSTRACT**

A circuit includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor, coupled between a supply voltage and the EL device, includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor, coupled between the first node and the second node, is configured to reset the gate of the transistor to the supply voltage in response to a first control signal. The second capacitor, including a first end coupled to the second node and a second end to receive a second control signal, is configured to establish at the first terminal of the transistor a compensation voltage associated with a threshold voltage of the transistor in response to the second control signal. The transistor is configured to pass a current through the EL device. The current has a magnitude independent of the threshold voltage of the transistor.



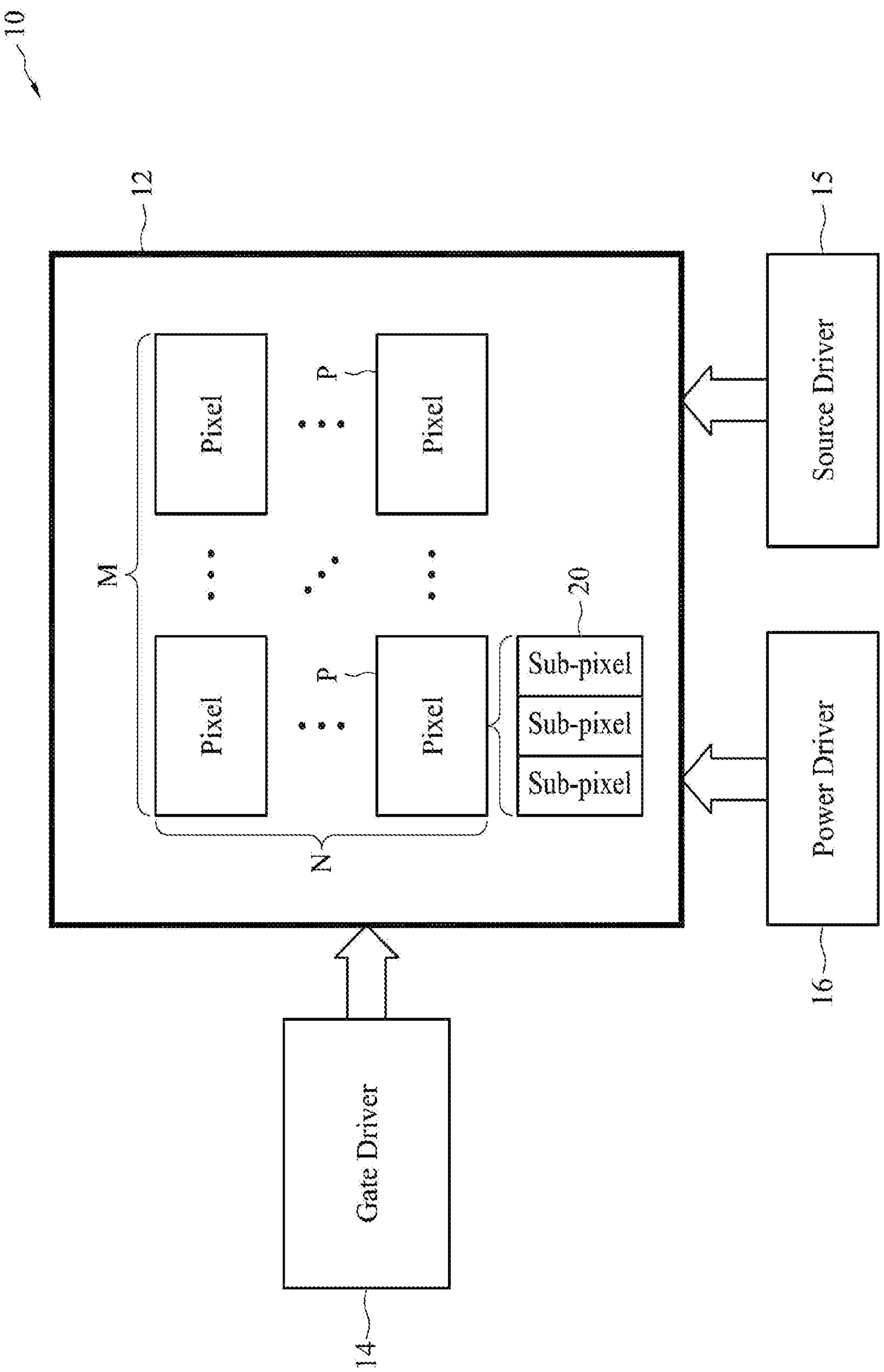

10
12
Pixel
P
Pixel
M
Pixel
P
Pixel
N
20
Sub-pixel
Sub-pixel
Sub-pixel
Source Driver
15
Power Driver
16
Gate Driver
14

FIG. 1

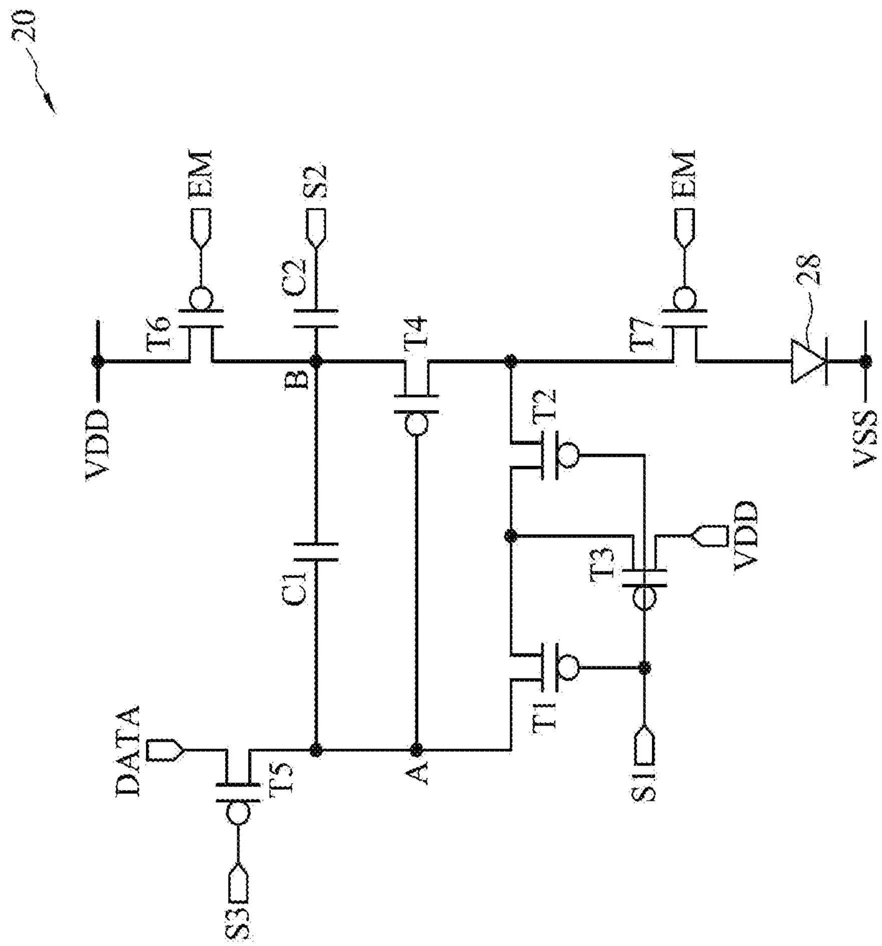


FIG. 2

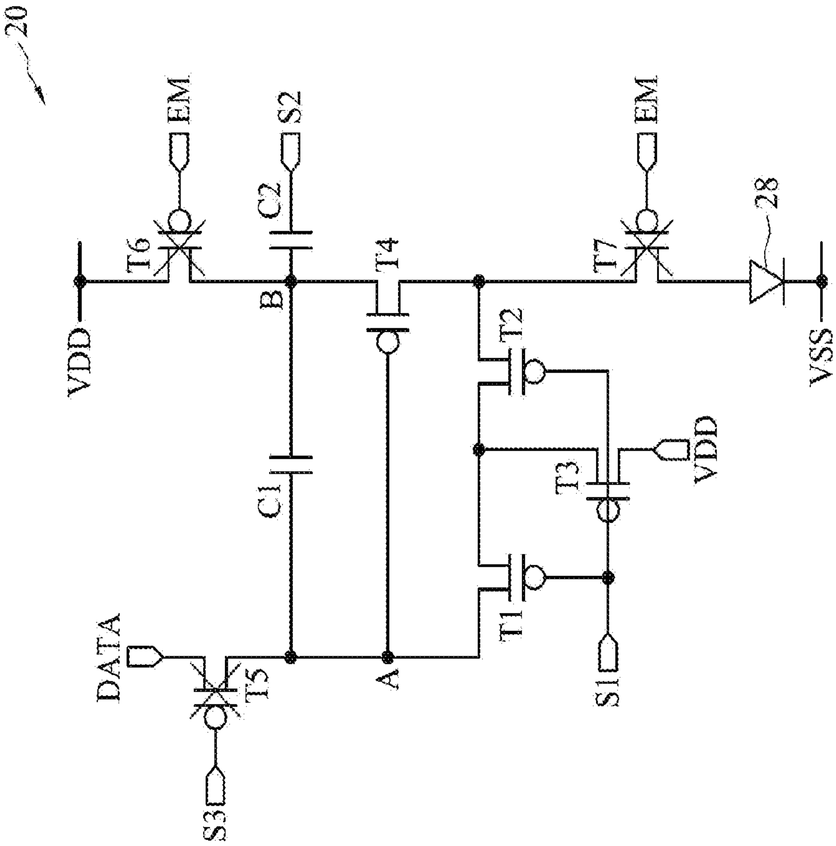

20
VDD
T6
EM
B
C2
S2
T4
T7
EM
28
VSS
T2
C1
T3
VDD
DATA
T5
A
T1
S1
S3

FIG. 3B

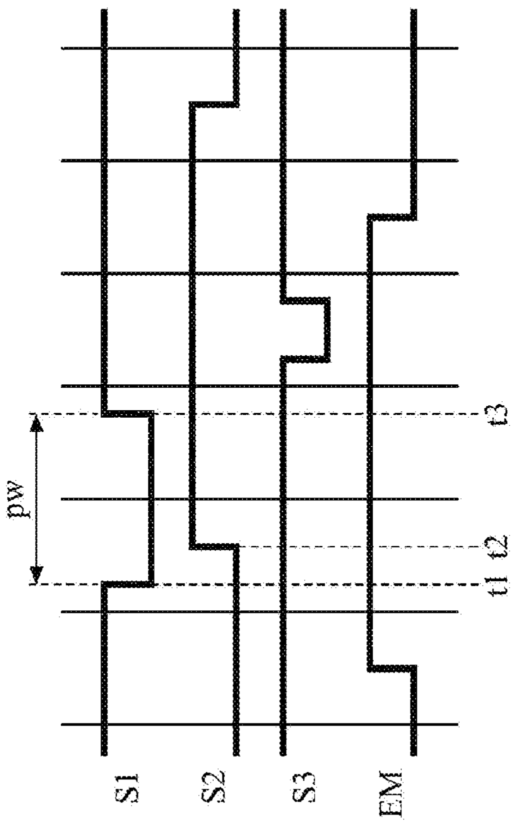

pw
t1 t2
t3
S1
S2
S3
EM

FIG. 3A

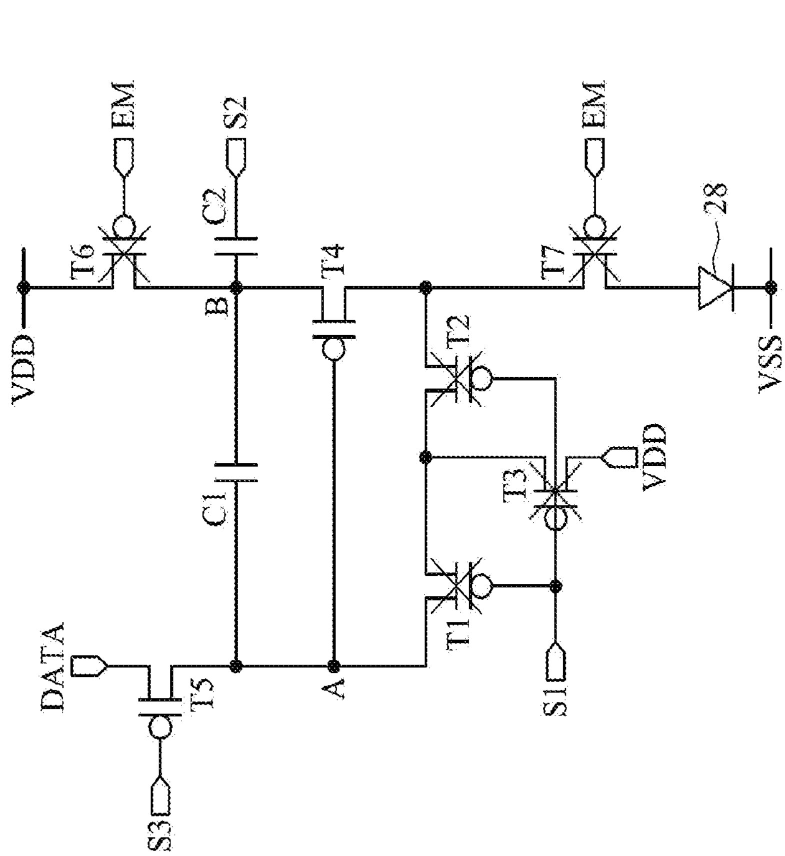

20
VDD
T6
EM
B
C2
S2
T4
T7
EM
28
VSS
T2
T3
VDD
C1
DATA
T5
A
T1
S1
S3

FIG. 4B

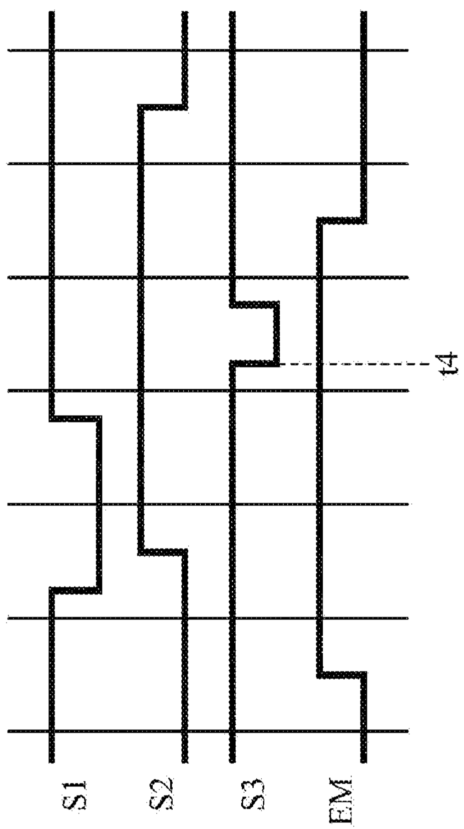

S1
S2
S3
EM
t4

FIG. 4A

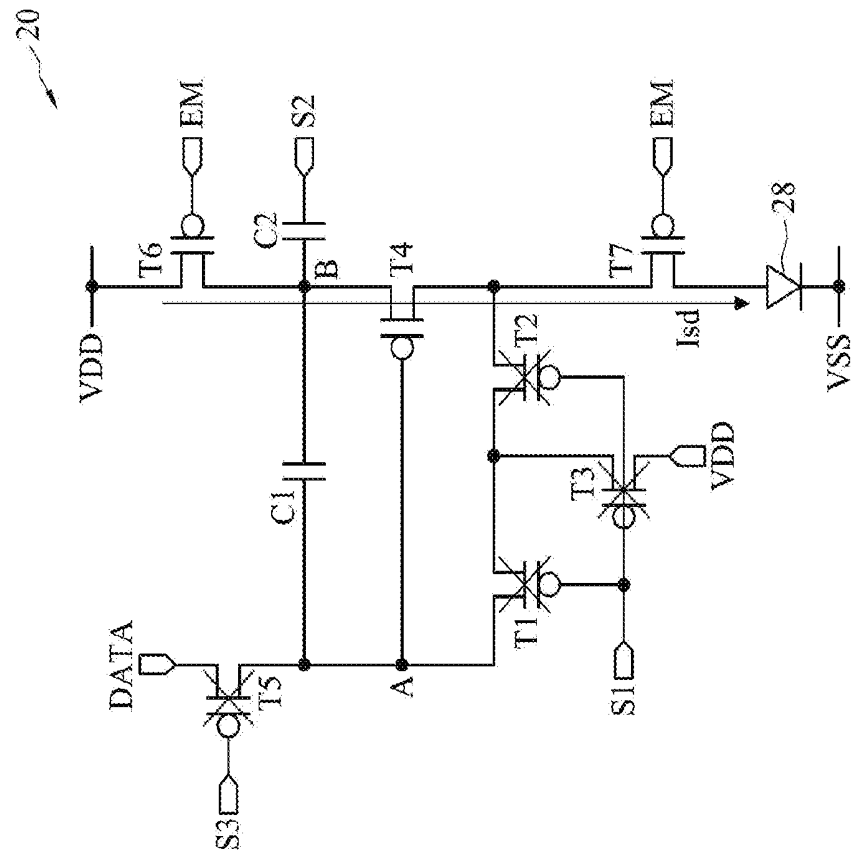

20
VDD
T6
EM
C2
S2
B
T4
T7
EM
28
Isd
VSS
C1
T2
T3
VDD
T1
S1
A
DATA
T5
S3

FIG. 5B

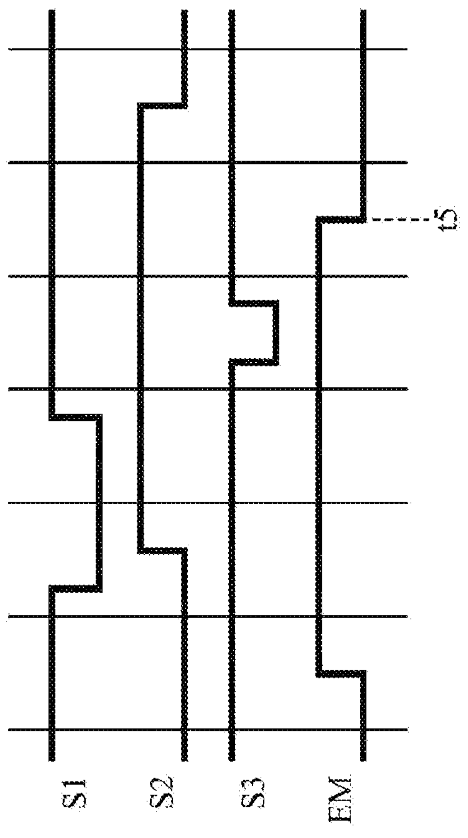
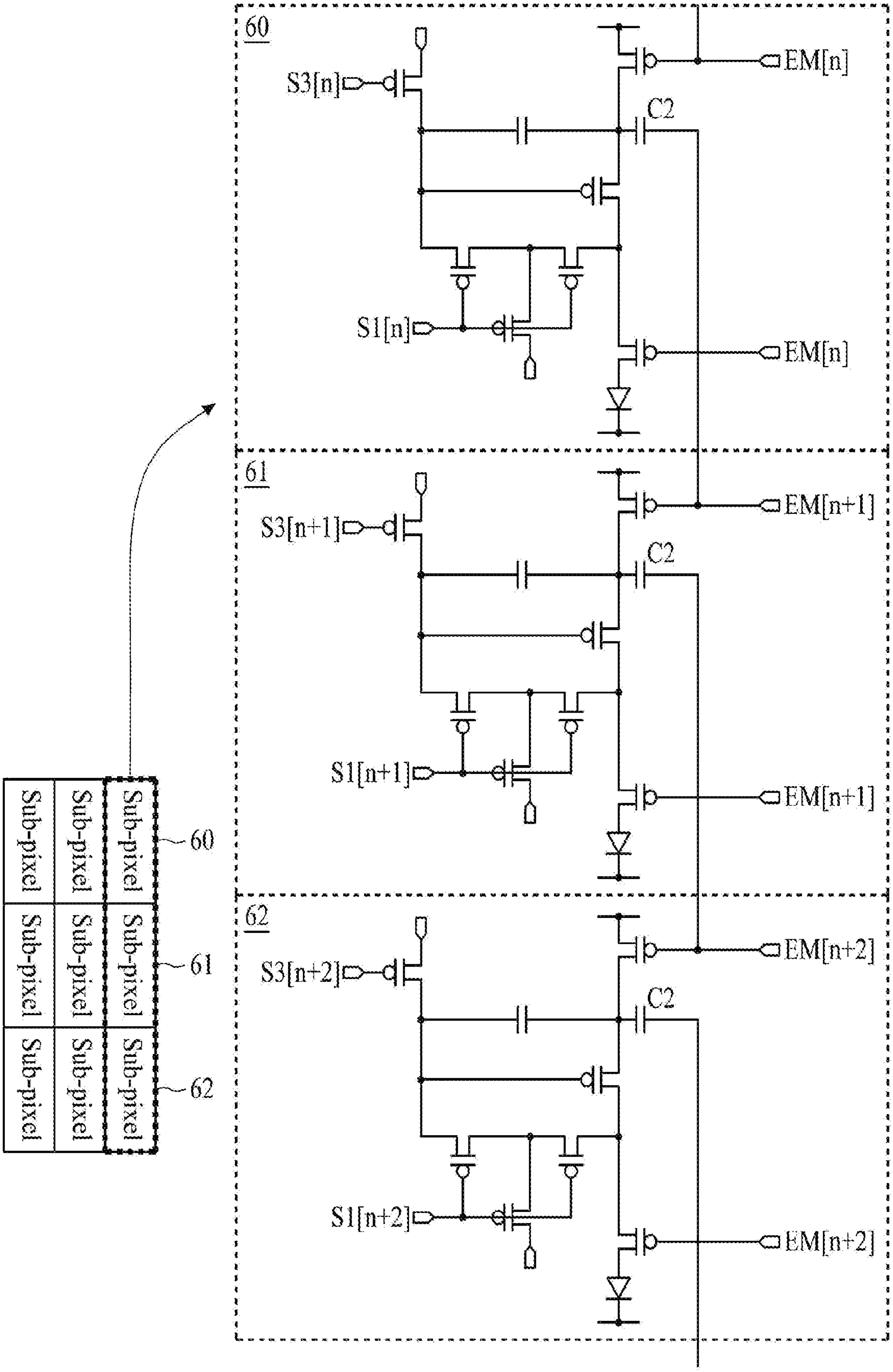

S1
S2
S3
EM
t5

FIG. 5A



60
S3[n]
EM[n]
C2
S1[n]
EM[n]
61
S3[n+1]
EM[n+1]
C2
S1[n+1]
EM[n+1]
62
S3[n+2]
EM[n+2]
C2
S1[n+2]
EM[n+2]
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
Sub-pixel
60
61
62

FIG. 6

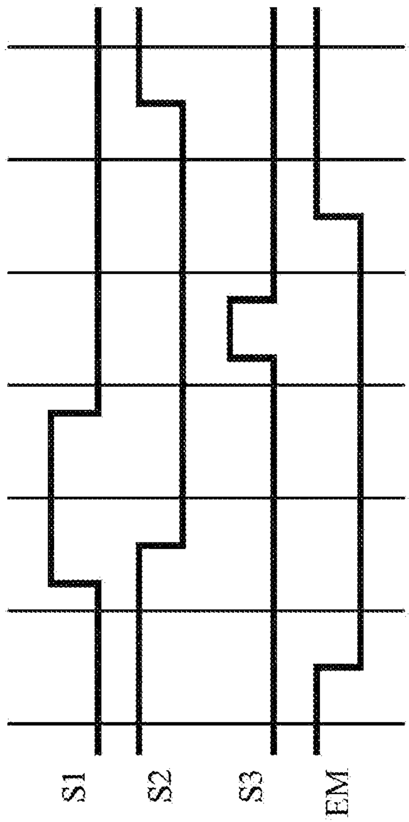

S1
S2
S3
EM

FIG. 7B

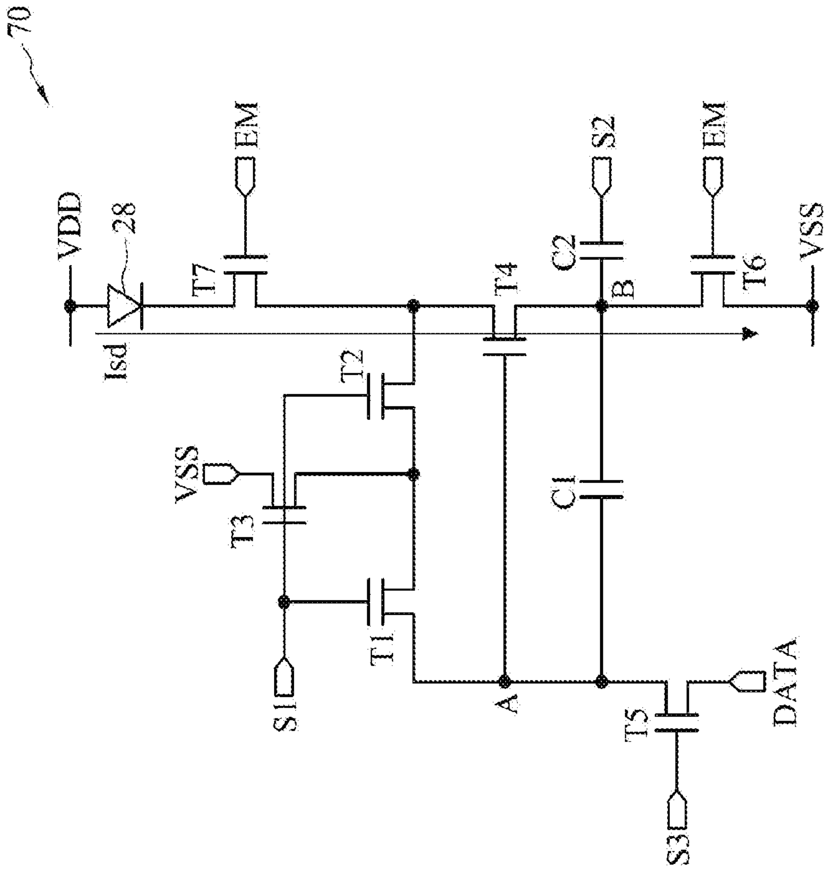

70
VDD
28
Isd
T7
EM
T4
T2
VSS
T3
T1
S1
A
C2
S2
B
T6
EM
VSS
C1
T5
DATA
S3

FIG. 7A

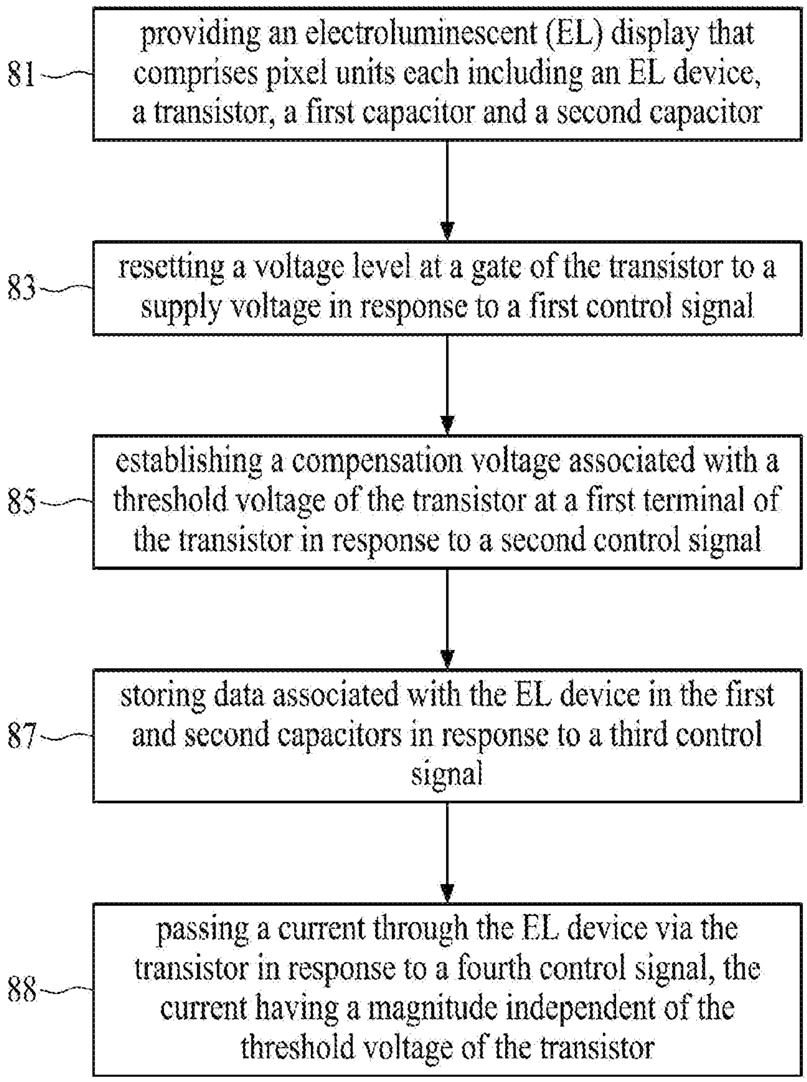

81
providing an electroluminescent (EL) display that comprises pixel units each including an EL device, a transistor, a first capacitor and a second capacitor
83
resetting a voltage level at a gate of the transistor to a supply voltage in response to a first control signal
85
establishing a compensation voltage associated with a threshold voltage of the transistor at a first terminal of the transistor in response to a second control signal
87
storing data associated with the EL device in the first and second capacitors in response to a third control signal
88
passing a current through the EL device via the transistor in response to a fourth control signal, the current having a magnitude independent of the threshold voltage of the transistor

FIG. 8

PIXEL CIRCUIT AND ELECTROLUMINESCENT DISPLAY COMPRISING THE PIXEL CIRCUIT

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. provisional application Ser. No. 62/421,435, filed Nov. 14, 2016, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND

[0002] An electroluminescent (EL) display, such as an active matrix organic light emitting diode (AMOLED) display, may include an array of pixels. Each of the pixels may include an EL device, a switching transistor for transfer data that contains information on luminescence, and a driving transistor for driving the EL device to emit light according to the data. While such EL display enjoys the benefit of relatively low power consumption, display non-uniformity may exist among pixels due to process factors in semiconductor manufacturing. It may thus be desirable to have a circuit that solves the problem.

SUMMARY

[0003] Embodiments of the present invention provide a circuit that includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor, coupled between a supply voltage and the EL device, includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor, coupled between the first node and the second node, is configured to reset the gate of the transistor to the supply voltage in response to a first control signal. The second capacitor, including a first end coupled to the second node and a second end to receive a second control signal, is configured to establish at the first terminal of the transistor a compensation voltage associated with a threshold voltage of the transistor in response to the second control signal. The transistor is configured to pass a current through the EL device. The current has a magnitude independent of the threshold voltage of the transistor.

[0004] In an embodiment, the circuit further includes a transistor configured to provide the supply voltage to the gate of the transistor in response to the first control signal.

[0005] In another embodiment, the circuit further includes a transistor configured to receive data associated with the EL device in response to a third control signal.

[0006] In yet another embodiment, the circuit further includes a transistor configured to allow the current to pass through the EL device in response to a fourth control signal.

[0007] In still another embodiment, the magnitude of the current is a function of a capacitance each of the first and second capacitors.

[0008] In yet still another embodiment, the transistor includes a p-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C2}{C1 + C2} \times (VDD - Vdata)\right]^2$$

[0009] where Isd represents the magnitude of the current, k is a constant, C1 and C2 represent capacitances of the first and second transistors, respectively, VDD represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

[0010] In still yet another embodiment, the transistor includes an n-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS)\right]^2$$

[0011] where Isd represents the magnitude of the current, k is a constant, C1 and C2 represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

[0012] In an embodiment, a pulse width of the first control signal substantially equals a frame time.

[0013] Some embodiments of the present invention provide an electroluminescent display that includes an array of pixel units. Each of the pixel units includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor, coupled between a supply voltage and the EL device, includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor, coupled between the first node and the second node, is configured to reset the gate of the transistor to the supply voltage in response to a first control signal. The second capacitor, including a first end coupled to the second node and a second end to receive a second control signal, is configured to establish at the first terminal of the transistor a compensation voltage associated with a threshold voltage of the transistor in response to the second control signal. The transistor is configured to pass a current through the EL device. The current has a magnitude independent of the threshold voltage of the transistor.

[0014] Embodiments of the present invention also provide a method of voltage compensation in an electroluminescent (EL) display that includes an array of pixel units each including an EL device, a transistor, a first capacitor and a second capacitor. The method comprises resetting a voltage level at a gate of the transistor to a supply voltage in response to a first control signal, establishing a compensation voltage associated with a threshold voltage of the transistor at a first terminal of the transistor in response to a second control signal, storing data associated with the EL device in the first and second capacitors in response to a third control signal, and passing a current through the EL device via the transistor in response to a fourth control signal. The current has a magnitude independent of the threshold voltage the transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0016] FIG. 1 is a block diagram of a display, in accordance with an embodiment.

[0017] FIG. 2 is a circuit diagram of a sub-pixel unit in the display illustrated in FIG. 1, in accordance with an embodiment.

[0018] FIGS. 3A and 3B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a first phase, in accordance with some embodiments.

[0019] FIGS. 4A and 4B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a second phase, in accordance with some embodiments.

[0020] FIGS. 5A and 5B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a third phase, in accordance with some embodiments.

[0021] FIG. 6 is a diagram of a circuit structure of sub-pixel units, in accordance with some embodiments.

[0022] FIG. 7A is a circuit diagram of a sub-pixel unit in a display, in accordance with another embodiment.

[0023] FIG. 7B is a waveform diagram of control signals for operating the circuit illustrated in FIG. 7A, in accordance with some embodiments.

[0024] FIG. 8 is a flow diagram showing a method of voltage compensation in an electroluminescent display.

DETAILED DESCRIPTION

[0025] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0026] Further, it will be understood that when an element is referred to as being "connected to" or "coupled to" another element, it may be directly connected to or coupled to the other element, or intervening elements may be present.

[0027] In the below description, a signal is asserted with a logical high value to activate a corresponding device when the device is active high. In contrast, the signal is deasserted with a low logical value to deactivate the corresponding device. When the device is active low, however, the signal is asserted with a low logical value to activate the device, and is deasserted with a high logical value to deactivate the device.

[0028] FIG. 1 is a block diagram of a display 10, in accordance with an embodiment. The display 10 may include an electroluminescent (EL) display, for example, an active matrix organic light emitting diode (AMOLED) display.

[0029] Referring to FIG. 1, the display 10 includes an active area 12, a gate driver 14 and a source driver 15. The active area 12 includes an array of pixel units P arranged in, for example, an N×M matrix. The gate driver 14 provides control signals S1, S2, S3 and EM through N scan lines to the N rows of pixel units. The source driver 15 provides data to a selected pixel of the M columns of pixel units. Moreover, a power driver 16 provides supply voltages in a power rail of VDD and VSS to the active area 12. In an embodiment, VDD is approximately five volts (5V), and VSS is approximately −5V.

[0030] Each pixel unit P in the active area 12 includes three sub-pixel units, which may be used to display color red (R), color green (G) and color blue (B). In other embodiments, for example, in a sub-pixel rendering (SPR) sensor, the number of sub-pixel units is not limited to three. In the present embodiment, the three sub-pixels are arranged along the row direction. Accordingly, the number of data lines for the source driver 15 is 3×M.

[0031] FIG. 2 is a circuit diagram of an exemplary sub-pixel unit 20 in the display 10 illustrated in FIG. 1, in accordance with an embodiment.

[0032] Referring to FIG. 2, the circuit includes an EL device 28, transistors T1 to T7, a first capacitor C1 and a second capacitor C2. The EL device 28 includes, for example, a current-driven element that may include an organic light emitting diode (OLED), a micro LED or a quantum dot LED (QLED). The first capacitor C1 and the second capacitor C2 serve as storage capacitors. The transistor T4 serves as a driving transistor to drive the EL device 28 according to data stored in the capacitors C1 and C2. In the present embodiment, each of the transistors T1 to T7 includes a p-type thin film transistor (TFT) or a p-type metal-oxide-semiconductor (PMOS) transistor.

[0033] A gate of the transistor T1 receives a first control signal S1. A drain of the transistor T1 is coupled to a first node A. In addition, a gate of the transistor T3 also receives the first control signal S1. A source of the transistor T3 receives a supply voltage VDD. A drain of the transistor T3 is coupled to a source of the transistor T1. Persons having ordinary skill in the art will understand that drain and source terminals of a MOS transistor may be interchangeable, depending on voltage levels applied thereto.

[0034] Moreover, a gate of the transistor T2 also receives the first control signal S1. A source of the transistor T2 is coupled to the source of the transistor T1 and hence the drain of the transistor T3. A gate of the transistor T4 is coupled to the first node A and hence the drain of the transistor T1. A source of the transistor T4 is coupled to a second node B. A drain of the transistor T4 is coupled to a drain of the transistor T2.

[0035] The first capacitor C1 is coupled between the first node A and the second node B. In addition, the second capacitor C2 has a first end coupled to the second node B, and a second end configured to receive a second control signal S2.

[0036] Furthermore, a gate of the transistor T5 receives a third control signal S3. A source of the transistor T5 receives data (labeled "DATA") on a corresponding data line from the source driver 15. A drain of the transistor T5 is coupled to the first node A and hence the gate of the transistor T4 and the drain of the transistor T1. In addition, a gate each of the transistors T6 and T7 receives a fourth control signal EM. A source of the transistor T6 receives VDD. A drain of the transistor T6 is coupled to the second node B and hence the source of the transistor T4. Moreover, a source of the transistor T7 is coupled to the drain each of the transistors T2 and T4. A drain of the transistor T7 is coupled to an anode of the EL device 28. A cathode of the EL device 28 receives another supply voltage VSS.

[0037] FIGS. **3**A and **3**B are diagrams showing a method of operating the circuit **20** illustrated in FIG. **2** in a first phase, in accordance with some embodiments.

[0038] Referring to FIG. **3**A, the control signals S**1**, S**3** and EM are configured to be active low in view of the p-type transistors T**1** to T**7**. At time t**1**, the first control signal S**1** is asserted at a falling edge, the second control signal S**2** is kept at a low logical level, and the third and fourth control signals S**3** and EM at a high logical level are not asserted. As a result, referring to FIG. **3**B, the transistors T**1**, T**2** and T**3** are turned on, while the transistors T**5** to T**7** are turned off (a cross sign "X" labeled). Since the transistors T**1** and T**3** are turned on, a voltage level at the first node A, denoted as VA, is pulled high to VDD. Moreover, in a previous phase (a third phase to be discussed in FIGS. **5**A and **5**B), a voltage level at node B, denoted as VB, is VDD (as the transistor T**6** is turned on) and is kept initially in the first phase. Since a voltage level at the gate and source (denoted as Vg and Vs, respectively) of the driving transistor T**4** is VDD, the transistor T**4** is turned off.

[0039] At time t**2**, the second control signal S**2** becomes logically high, the first control signal S**1** is kept at a low logical level, and the third and fourth control signals S**3** and EM are not asserted. With the transition of the second control signal S**2** from low to high at time t**2**, by the coupling function of the second capacitor C**2**, VB initially at VDD is pulled up to a level higher than VDD+|Vth4|, where |Vth4| is the threshold voltage of the transistor T**4**. The transistor T**4** is then turned on. As a result, during the first phase, VA (or Vg of the transistor T**4**) is reset to VDD. Moreover, a compensation voltage is established at VB (or Vs of the transistor T**4**). VB or Vs can reach a desirable value of VDD+|Vth4| by means of adjusting a pulse width pw of the first control signal S**1**. The pulse width pw of the first control signal S**1** is a time period that the first control signal S**1** stays activated. For example, in the present embodiment as illustrated in FIG. **3**A, the pulse width pw of the first control signal S**1** is from time t**1** to t**3**. In the present embodiment, |Vth4| associated with the driving transistor T**4** represents a compensation voltage. The time for establishing the compensation voltage, hereinafter "the compensation time," is positively proportional to the pulse width pw of the first control signal S**1**. Moreover, the pulse width pw of the first control signal S**1** is not limited by the resolution of the display **10**. As the compensation time becomes longer, the voltage level of VB reaches closer to the saturation voltage of the second capacitor C**2**, which enhances the display quality of the display **10**. Effectively, the compensation time, or the pulse width pw, can be as long as a frame time.

[0040] FIGS. **4**A and **4**B are diagrams showing a method of operating the circuit **20** illustrated in FIG. **2** in a second phase, in accordance with some embodiments.

[0041] Referring to FIG. **4**A, at time t**4**, the third control signal S**3** is asserted at a falling edge, the second control signal S**2** is kept at a high logical level, and the first and fourth control signals S**1** and EM are not asserted. As a result, referring to FIG. **4**B, the transistor T**5** is turned on, the transistors T**1** to T**3** are turned off, and the transistors T**6** and T**7** are kept at an off state. Since the transistor T**5** is turned on, data is written to the first node A. Accordingly, VA (Vg) becomes Vdata. In addition, as VA changes from VDD (first phase) to Vdata (second phase), by the coupling function of the first capacitor C**1**, VB becomes

$$VDD + |Vth4| + \left[\frac{C1}{C1 + C2} \times (Vdata - VDD)\right].$$

For convenience, a same reference numeral or label for a capacitor is also used for its capacitance throughout the disclosure, and vice versa. For example, while the reference label "C**1**" as above mentioned refers to the first capacitor, it may also represent the capacitance of the first capacitor.

[0042] FIGS. **5**A and **5**B are diagrams showing a method of operating the circuit **20** illustrated in FIG. **2** in a third phase, in accordance with some embodiments.

[0043] Referring to FIG. **5**A, at time t**5**, the fourth control signal EM is asserted at a falling edge, the second control signal S**2** is kept at a high logical level, and the first and third control signals S**1** and S**3** are not asserted. As a result, referring to FIG. **5**B, the transistors T**6** and T**7** are turned on, the transistor T**5** is turned off, and the transistors T**1** to T**3** are kept at an off state. Since the transistor T**6** is turned on, VB (Vs) is pulled to VDD from

$$VDD + |Vth4| + \left[\frac{C1}{C1 + C2} \times (Vdata - VDD)\right].$$

By the function of the first capacitor C**1**, VA (Vg) becomes

$$Vdata - \left\{|Vth4| + \left[\frac{C1}{C1 + C2} \times (Vdata - VDD)\right]\right\}.$$

[0044] Moreover, a current Isd flows from supply power VDD through the EL device **28** to VSS via the transistors T**6**, T**4** and T**7**. The current Isd can be expressed in equation (1) below.

$$|Isd| = k \times (|Vsg| - |Vth4|)^2 \qquad \text{equation (1)}$$

[0045] where k is a constant, Vsg represents a source to gate voltage of the transistor T**4**.

[0046] Since

$$Vsg = Vs - Vg = VB - VA = |Vth4| + \left[\frac{C2}{C1 + C2} \times (VDD - Vdata)\right],$$

by substituting the result into equation (1), the current Isd is rewritten as follows.

$$|Isd| = k \times \left[\frac{C2}{C1 + C2} \times (VDD - Vdata)\right]^2 \qquad \text{equation (2)}$$

[0047] The current Isd is independent of the threshold voltage of the transistor T**4**. Since equation (2) is free of the Vth term, the display quality of the display **10** is enhanced.

[0048] FIG. **6** is a diagram of a circuit structure of sub-pixel units, in accordance with some embodiments. Referring to FIG. **6**, the circuit structure is similar to that described and illustrated with reference to FIG. **2** except that, for example, sub-pixel units arranged along the column direction are configured to receive a fourth control signal EM, that is provided to an immediately adjacent sub-pixel unit on a next row, as a second control signal **S2**. For discussion, only exemplary sub-pixel units **60**, **61** and **62** are shown. As a result, a second control signal S2[*n*] that would otherwise be provided to a sub-pixel unit on an n-th row as in FIG. **3**A, **4**A or **5**A is replaced by a fourth control signal EM[n+1] provided to a sub-pixel unit on an (n+1)-th row. Specifically, for the sub-pixel unit **60**, a fourth control signal EM[n+1] provided to the sub-pixel unit **61** also serves as a second control signal coupled to the second terminal of the second capacitor C**2** in the sub-pixel unit **60**. In addition, for the sub-pixel unit **61**, a fourth control signal EM[n+2] provided to the sub-pixel unit **62** also serves as a second control signal coupled to the second terminal of the second capacitor C**2** in the sub-pixel unit **61**. Effectively, the control mechanism is simplified.

[0049] FIG. **7**A is a circuit diagram of a sub-pixel unit **70** in a display, in accordance with another embodiment.

[0050] Referring to FIG. **7**A, the circuit is similar to the circuit described and illustrated with reference to FIG. **2** except that, for example, n-type TFTs or NMOS transistors replace the p-type TFTs or PMOS transistors T**1** to T**7** in FIG. **2**.

[0051] Specifically, a gate of the transistor T**1** receives a first control signal S**1**. A drain of the transistor T**1** is coupled to a first node A. In addition, a gate of the transistor T**3** also receives the first control signal S**1**. A source of the transistor T**3** receives VSS. A drain of the transistor T**3** is coupled to a source of the transistor T**1**. Moreover, a gate of the transistor T**2** also receives the first control signal S**1**. A source of the transistor T**2** is coupled to the source of the transistor T**1** and hence the drain of the transistor T**3**. A gate of the transistor T**4** is coupled to the first node A and hence the drain of the transistor T**1**. A source of the transistor T**4** is coupled to a second node B. A drain of the transistor T**4** is coupled to a drain of the transistor T**2**.

[0052] The first capacitor C**1** is coupled between the first node A and the second node B. In addition, the second capacitor C**2** has a first terminal coupled to the second node B, and a second terminal to receive a second control signal S**2**.

[0053] Furthermore, a gate of the transistor T**5** receives a third control signal S**3**. A drain of the transistor T**5** receives data (labeled "DATA") on a corresponding data line from the source driver **15**. A source of the transistor T**5** is coupled to the first node A and hence the gate of the transistor T**4** and the drain of the transistor T**1**. In addition, a gate each of the transistors T**6** and T**7** receives a fourth control signal EM. A source of the transistor T**6** receives VSS. A drain of the transistor T**6** is coupled to the second node B and hence the source of the transistor T**4**. Moreover, a source of the transistor T**7** is coupled to the drain each of the transistors T**2** and T**4**. A drain of the transistor T**7** is coupled to a cathode of the EL device **28**. An anode of the EL device **28** is coupled to VDD.

[0054] FIG. **7**B is a timing diagram for operating the circuit illustrated in FIG. **7**A, in accordance with some embodiments.

[0055] Referring to FIG. **7**B, the control signals S**1**, S**3** and EM are similar to those described and illustrated with reference to FIG. **3**A, **4**A or **5**A except that, for example, the control signals S**1**, S**3** and EM in FIG. **7**B are active high or asserted at a rising edge in view of n-type transistors T**1** to T**7**, while the second control signal S**2** has an inverted phase as compared to that illustrated in FIG. **3**A, **4**A or **5**A.

[0056] The current Isd flowing through the EL device **28** in FIG. **7**A can be expressed in equation (3) below.

$$|Isd| = k \times (|Vgs| - |Vth4|)^2 = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS)\right]^2 \quad \text{equation (3)}$$

[0057] Similarly, the current Isd is independent of the threshold voltage of the transistor T**4**. Since equation (3) is free of the Vth term, the display quality of the display **10** is enhanced. Moreover, the simplified control mechanism as described and illustrated with reference to FIG. **6** is also applicable to the sub-pixel unit **70** in FIG. **7**A.

[0058] FIG. **8** is a flow diagram showing a method of voltage compensation in an electroluminescent display.

[0059] Referring to FIG. **8**, in operation **81**, an electroluminescent (EL) display is provided. The EL display includes an array of pixel units each including an EL device, a transistor, a first capacitor and a second capacitor.

[0060] Next, in operation **83**, a voltage level at a gate of the transistor is reset to a supply voltage in response to a first control signal.

[0061] In operation **85**, a compensation voltage associated with a threshold voltage of the transistor is established at a first terminal of the transistor in response to a second control signal.

[0062] In operation **87**, data associated with the EL device is stored in the first and second capacitors in response to a third control signal.

[0063] Subsequently, in operation **88**, a current is passed through the EL device via the transistor in response to a fourth control signal. The current has a magnitude independent of the threshold voltage the transistor.

[0064] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A circuit, comprising:

an electroluminescent (EL) device;

a transistor, coupled between a supply voltage and the EL device, including a gate coupled to a first node and a first terminal coupled to a second node;

a first capacitor, coupled between the first node and the second node, being configured to reset the gate of the transistor to the supply voltage in response to a first control signal; and

a second capacitor including a first end coupled to the second node and a second end to receive a second control signal, the second capacitor being configured to establish at the first terminal of the transistor a compensation voltage associated with a threshold voltage of the transistor in response to the second control signal, wherein the transistor is configured to pass a current through the EL device, the current having a magnitude being independent of the threshold voltage of the transistor.

2. The circuit according to claim **1** further comprising a transistor configured to provide the supply voltage to the gate of the transistor in response to the first control signal.

3. The circuit according to claim **1** further comprising a transistor configured to receive data associated with the EL device in response to a third control signal.

4. The circuit according to claim **1** further comprising a transistor configured to allow the current to pass through the EL device in response to a fourth control signal.

5. The circuit according to claim **1**, wherein the magnitude of the current is a function of a capacitance each of the first and second capacitors.

6. The circuit according to claim **1**, wherein the transistor includes a p-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C2}{C1 + C2} \times (VDD - Vdata)\right]^2$$

where Isd represents the magnitude of the current, k is a constant, C**1** and C**2** represent capacitances of the first and second transistors, respectively, VDD represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

7. The circuit according to claim **1**, wherein the transistor includes an n-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS)\right]^2$$

where Isd represents the magnitude of the current, k is a constant, C**1** and C**2** represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

8. The circuit according to claim **1**, wherein a pulse width of the first control signal substantially equals a frame time.

9. An electroluminescent display, comprising:

an array of pixel units, each of the pixel units comprising:

an electroluminescent (EL) device;

a transistor, coupled between a supply voltage and the EL device, including a gate coupled to a first node and a first terminal coupled to a second node;

a first capacitor, coupled between the first node and the second node, being configured to reset the gate of the transistor to the supply voltage in response to a first control signal; and

a second capacitor including a first end coupled to the second node and a second end to receive a second control signal, the second capacitor being configured to establish at the first terminal of the transistor a compensation voltage associated with a threshold voltage of the transistor in response to the second control signal,

wherein the transistor is configured to pass a current through the EL device, the current having a magnitude being independent of a threshold voltage of the transistor.

10. The electroluminescent display according to claim **9** further comprising a transistor configured to provide the supply voltage to the gate of the transistor in response to the first control signal.

11. The electroluminescent display according to claim **9** further comprising a transistor configured to receive data associated with the EL device in response to a third control signal.

12. The electroluminescent display according to claim **9** further comprising a transistor configured to allow the current to pass through the EL device in response to a fourth control signal.

13. The electroluminescent display according to claim **12**, wherein the array of pixel units includes a first pixel unit on an N-th row of the array and a second pixel unit on an (N+1)-th row of the array and immediately adjacent to the first pixel unit, N being a natural number, and wherein the fourth control signal provided to the second pixel unit serves as the second control signal for the first pixel unit.

14. The electroluminescent display according to claim **9**, wherein the magnitude of the current is a function of a capacitance each of the first and second capacitors.

15. The electroluminescent display according to claim **9**, wherein the transistor includes a p-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C2}{C1 + C2} \times (VDD - Vdata)\right]^2$$

where Isd represents the magnitude of the current, k is a constant, C**1** and C**2** represent capacitances of the first and second transistors, respectively, VDD represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

16. The electroluminescent display according to claim **9**, wherein the transistor includes an n-type transistor, and the current is expressed as:

$$|Isd| = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS)\right]^2$$

where Isd represents the magnitude of the current, k is a constant, C**1** and C**2** represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and Vdata represents a voltage level of data associated with the EL device.

17. The electroluminescent display according to claim **9**, wherein a pulse width of the first control signal substantially equals a frame time.

18. A method of voltage compensation in an electroluminescent (EL) display that comprises an array of pixel units each including an EL device, a transistor, a first capacitor and a second capacitor, the method comprising:

resetting a voltage level at a gate of the transistor to a supply voltage in response to a first control signal;

establishing a compensation voltage associated with a threshold voltage of the transistor at a first terminal of the transistor in response to a second control signal;

storing data associated with the EL device in the first and second capacitors in response to a third control signal; and passing a current through the EL device via the transistor in response to a fourth control signal, the current having a magnitude independent of the threshold voltage the transistor.

19. The method according to claim **18**, wherein the array of pixel units includes a first pixel unit on an N-th row of the array and a second pixel unit on an (N+1)-th row of the array and immediately adjacent to the first pixel unit, N being a natural number, further comprising:

using the fourth control signal provided to the second pixel unit as the second control signal for the first pixel unit.

20. The method according to claim **19**, further comprising:

providing the first control signal having a pulse width substantially equal to a frame time.

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专利名称(译)	像素电路和电致发光显示器包括像素电路		
公开(公告)号	US20180137815A1	公开(公告)日	2018-05-17
申请号	US15/439420	申请日	2017-02-22
申请(专利权)人(译)	国际科技股份有限公司		
当前申请(专利权)人(译)	国际科技股份有限公司		
[标]发明人	CHENG SHIH SONG		
发明人	CHENG, SHIH-SONG		
IPC分类号	G09G3/3233 H01L27/32 H01L51/50		
CPC分类号	G09G3/3233 H01L27/3211 H01L27/3248 H01L51/5036 G09G2310/0278 G09G2300/0452 G09G2300/043 G09G2300/0814 G09G2300/0842 G09G2300/0443 G09G3/3225 G09G3/3258 G09G3/3266 G09G3/3275 G09G3/3674 G09G3/3685 G09G2300/0809 H01L27/0207 H01L27/088 H01L29/0847 G06F3/1446 G09G3/3208 G09G3/3611 G09G2300/026 G09G2300/0439 G09G2330/02 G09G3/2092 G09G3/30 G09G2300/0819 G09G2320/0204 G09G2320/0233 G09G2320/029 G09G2320/045 H01L23/528 H01L27/3244 H01L29/41733 H01L29/78		
优先权	62/421435 2016-11-14 US		
其他公开文献	US10431142		
外部链接	Espacenet USPTO		

摘要(译)

电路包括电致发光（EL）器件，晶体管，第一电容器和第二电容器。耦合在电源电压和EL器件之间的晶体管包括耦合到第一节点的栅极和耦合到第二节点的第一端子。耦合在第一节点和第二节点之间的第一电容器被配置为响应于第一控制信号将晶体管的栅极重置为电源电压。包括耦合到第二节点的第一端和用于接收第二控制信号的第二端的第二电容器被配置为响应于所述晶体管的阈值电压而在晶体管的第一端建立与晶体管的阈值电压相关联的补偿电压第二控制信号。晶体管被配置为使电流通过EL器件。电流的大小与晶体管的阈值电压无关。